

PTO/SB/08a 07-05

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				FAX RECEIVED	
Sheet	1	of	10	Examiner Name	MAY 11 2006
				Attorney Docket Number	43876-144 OFFICE OF PETITIONS

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
DW	AA	US-4,852,098	07/25/1989	Brechard, et al.	—
	AB	US-4,875,161	10/17/1989	Lahti, et al.	—
	AC	US-4,949,294	08/14/1990	Wundergut, et al.	—
	AD	US-4,953,073	08/28/1990	Mousouris, et al.	—
	AE	US-4,959,779	09/25/1990	Weber, et al.	—
	AF	US-5,081,698	01/14/1992	Kohn	—
	AG	US-5,113,506	05/12/1992	Mousouris, et al.	—
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	AJ	US-5,161,247	11/03/1992	Murakami, et al.	—
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	AK	US-5,231,646	07/27/1993	Heath, et al.	—
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	AM	US-5,241,636	08/31/1993	Kohn	—
	AN	US-5,280,598	01/18/1994	Ozaki, et al.	—
	AO	US-5,487,024	01/23/1996	Girardeau, Jr.	—
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V	AQ	US-5,533,185	07/02/1996	Lentz, et al.	—
	AR	US-5,590,363	12/31/1996	Idr, et al.	—
DW	AS	US-5,600,814	02/04/1997	Gahan, et al.	—

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Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Country Code ² Number " Kind Code ² (if known)			
DW	AT	WO 93/11500	—	—	—

Examiner Signature	/Daniel Washburn/	Date Considered	08/18/2006
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				FAX RECEIVED	
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Sheet	2	of	10	Examiner Name	Mackly Monestelle
				Attorney Docket Number	43876-144

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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issued number(s), publisher, city and/or country where published.			
AU		IEEE Draft Standard for "Scalable Coherent Interface Low-Voltage Differential Signal Specifications and Packer Encoding". IEEE Standards Department, P1596.3/D0.15 (Mar. 1992) (50006DOC018330 - 563)			/
AV		IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)," IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X (May 1995) (50006DOC018413 - 529)			/
AW		Gove, Koen et al., "MIPS RISC Architecture," Prentice Hall (1995) (50006DOC018526 - 848)			/
DW	AX	IBM, "The PowerPC Architecture: A Specification For A New Family of RISC Processors," 2nd Ed., Morgan Kaufmann Publishers, Inc., (1994) (50006DOC019229 - 767)			/
	AY	Hewlett-Packard Co., "PA-RISC 1.1 Architecture and Instruction Set," Manual Part No. 09740-90039, (1990) (51056DOC018849 - 19228)			/
	AZ	MIPS Computer Systems, Inc., "MIPS R4000 User's Manual," Mfg. Part No. MB-00040, (1990) (51006DOC017026 - 621)			/
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	BC	Gove, "The Multimedia Video Processor (MVP): A Chip Architecture for Advanced DSP Applications," IEEE DSP Workshop, pp. 27-30 (October 2-5, 1994) (51056DOC015452 - 455)			/
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	BH	Bass et al., "The PA 7100LC Microprocessor: A Case Study of IC Design Decisions in a Competitive Environment," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 12-22 (April 1995) (51056DOC059283 - 289)			/
	BI	Bowers et al., "Development of a Low-Cost, High Performance, Multiuser Business Server System," Hewlett-Packard Journal, Vol. 46, No. 2, p. 79 (April 1995) (51056DOC059277 - 282)			/
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	BK	Gwynnap, "Digital MIPS Adds Multimedia Extensions," Microdesign Resources, pp. 24-28 (November 18, 1996) (51056DOC003454 - 459)			/
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Examiner Signature	/Daniel Washburn/	Dated Considered	08/18/2006
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Substitute for Form 1449A/PTO				Complete if Known	
				FAX RECEIVED	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Application Number 10/616,303 Filing Date July 10, 2003 MAY 11 2006 First Named Inventor Craig Hansen Group Art Unit 2676 Examiner Name Mackly Monestime	
				OFFICE OF PETITIONS	
Sheet	3	of	10	Attorney Docket Number 43876-144	

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

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Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ² Number ³ Kind Code ⁴ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

Examiner Signature	/Daniel Washburn/	Date Considered	08/18/2006
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Sheet	4	of	10	Examiner Name	Mackly Monestime
				Attorney Docket Number	43876-144

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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	
DW	BX	Lee, "Realtime MPEG Video via Software Decompression on a PA-RISC Processor," IEEE, pp. 186-92 (1995) (51056DOC007345 - 351)	/
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	CE	Diefendorff et al., "The Motorola 88110 Superscalar RISC Microprocessor," IEEE pp. 157-62 (1992) (51056DOC008746 - 751)	/
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	CR	Knapp et al., "Bulk Storage Applications in the ILLIAC IV System," ILLIAC IV Document No. 250, Center for Advanced Computation, University of Illinois at Urbana-Champaign (August 3, 1971) (51056DOC001647 - 656)	/
▼	CS	Awaga et al., "The µVP 64-bit Vector Coprocessor: A New Implementation of High-Performance Numerical Computation," IEEE Micro, Vol. 13, No. 5, pp. 24-36 (October 1993) (51056DOC011921 - 934)	/
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Examiner Signature	/Daniel Washburn/	Dated Considered	08/18/2006
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Sheet

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of

10

Complete if Known

Application Number	10/616,303
Filing Date	July 10, 2003
First Named Inventor	Craig Hansen
Group Art Unit	2676
Examiner Name	Mackly Moninger

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Attorney Docket Number 43876-144

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issnme number(s), publisher, city and/or country where published.	Td
DW	CU	Urhiyama et al., "The Gmicro/500 Superscalar Microprocessor with Branch Buffers," IEEE Micro (October 1993) (51056DOC000185 - 194)	1
	CV	Broughton et al., "The S-1 Project: Top-End Computer Systems for National Security Applications," (October 24, 1985) (51056DOC057368 - 607)	1
	CW	Farmwald et al., "Signal Processing Aspects of the S-1 Multiprocessor Project," SPIE Vol. 241, Real-Time Signal Processing (1980) (51056DOC072280 - 291)	1
	CX	Farmwald, "High Bandwidth Evaluation of Elementary Functions," IEEE Proceedings, 5th Symposium on Computer Arithmetic (1981) (51056DOC071029 - 034)	1
	CY	Gilben, "An Investigation of the Partitioning of Algorithms Across an MIMD Computing System," (February 1980) (51056DOC072244 - 279)	1
	CZ	Widdoes, "The S-1 Project: Developing High-Performance Digital Computers," IEEE Computer Society C(OMPCON Spring 1980 (December 11, 1979) (51056DOC071574 - 585)	1
	DA	Cornell, S-1 Uniprocessor Architecture SMA-4 (51056DOC036505 - 895)	1
	DB	The S-1 Project, January 1985, S-1 Technical Staff (51056DOC057368 - 607)	1
	DC	S-1 Architecture and Assembler SMA-4 Manual, December 19, 1979 (Preliminary Version) (51056DOC057608 - 918)	1
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	DF	C4 Technical Overview (September 23, 1993) (51056DOC017111 - 157)	1
	DG	Saturn Assembly Level Performance Tuning Guide (January 1, 1994) (51056DOC017369 - 376)	1
	DH	Saturn Differences from C Series (February 6, 1994) (51056DOC017150 - 157)	1
	DI	"Convex Adds GaAs System," Electronic News (June 20, 1994) (51056DOC019388 - 390)	1
	DJ	Convex Architecture Reference Manual, Sixth Edition (1992) (51056DOC016599 - 993)	1
	DK	Convex Assembly Language Reference Manual, First Edition (December 1991) (51056DOC015996 - 6598)	1
	DL	Convex Data Sheet C4/XA Systems, Convex Computer Corporation (51056DOC059235 - 236)	1
	DM	Saturn Overview (November 12, 1993) (51056DOC017111 - 157)	1
	DN	Convex Notebook containing various "Machine Descriptions" (51056DOC016994 - 7510)	1
	DO	"Convex C4/XA Offer 1 GFLOPS from GaAs Uniprocessor," Computergram International, June 15, 1994 (51056DOC019383)	1
	DP	Excerpt from Convex C4600 Assembly Language Manual, 1993 (51056DOC061441 - 443)	1
	DQ	Excerpt from "Advanced Computer Architectures - A Design Space Approach," Chapter 14.8, "The Convex C4/XA System" (51056DOC061453 - 459)	1
↓	DR	Convex C4600 Assembly Language Manual, First Edition, May 1995 (51056DOC064728 - 5299)	1
DW	DS	Alvarez et al., "A 450MHz PowerPC Microprocessor with Enhanced Instruction Set and Copper Interconnect," ISSCC (February 1999) (51056DOC071393 - 394)	1

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				Filing Date	July 10, 2003
				First Named Inventor	Craig Hansen
				Group Art Unit	2676
				Examiner Name	Mackiv Monesem
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DW	DT	Tyler et al., "Altivec™: Bringing Vector Technology to the PowerPC™ Processor Family," IEEE (February 1999) (51056DOC071035 - 042)	/
	DU	Altivec™ Technology Programming Environments Manual (1998) (51056DOC071043 - 392)	/
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EA		Kohn et al., "Introducing the Intel i860 64-Bit Microprocessor," IEEE Micro, pp. 15-30 (August 1989) (5156DOC070627 - 642)	/
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EC		Margulis, "i860 Microprocessor Architecture," Intel Corporation (1990) (51056DOC066610 - 7265 and 5156DOC069971 - 70626)	/
ED		Mizal et al., "MMX Technology Architecture Overview," Intel Technology Journal Q3 '97, pp. 1-12 (1997) (5156DOC070689 - 700)	/
EE		Patel et al., "Architectural Features of the i860 – Microprocessor RISC Core and On-Chip Caches," IEEE, pp. 385-90 (1989) (5156DOC070679 - 684)	/
EF		Rhodhamel, "The Bus Interface and Paging Units of the i860 Microprocessor," IEEE, pp. 380-84 (1989) (5156DOC070643 - 647)	/
EG		Perry, "Intel's Secret Is Out," IEEE Spectrum, pp. 22-28 (April 1989) (5156DOC070648 - 654)	/
EH		Sil et al., "An 80 MFLOPS Floating-Point Engine in the Intel i860 Processor," IEEE, pp. 374-79 (1989) (51056DOC072095 - 101)	/
EI		i860 XP Microprocessor Data Book, Intel Corporation (May 1991) (51056DOC067266 - 427)	/
EJ		Paragon User's Guide, Intel Corporation (October 1993) (51056DOC068802 - 9097)	/
EK		N15 Micro Architecture Specification, dated April 29, 1991 (50781DOC000001 - 982)	/
EL		N15 External Architecture Specification, dated October 17, 1990 (51056DOC017511 - 551)	/
EM		N15 External Architecture Specification, dated December 14, 1990 (50781DOC001442 - 509)	/
EN		N15 Product Requirements Document, dated December 21, 1990 (50781DOC001420 - 441)	/
EO		N15 Product Implementation Plan, dated December 21, 1990 (50781DOC001794 - 851)	/
EP		N12 Performance Analysis document version 2.0, dated September 21, 1990 (51056DOC072992 - 73027)	/
EQ		Hansen, "Architecture of a Broadband Mediaprocessor," IEEE COMPCON 96 (February 25-29, 1996) (MU0013276 - 283 and 51057DOC001825 - B31)	/
DW	ER	Mousouris et al., "Architecture of a Broadband MediaProcessor," Microprocessor Forum (1995) (MU0048611 - 630)	/

Examiner Signature	/Daniel Washburn/	Dated Considered	08/18/2006
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				FAX RECEIVED	
(use as many sheets as necessary)					
Sheet	7	of	10	Examiner Name	Mackly Mongomery
				Attorney Docket Number	43876-144

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS		
Examiner Initials*	Cite No. [†]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issued number(s), publisher, city and/or country where published.
DW	ES	Arnould et al., "The Design of Nectar A Network Backplane for Heterogeneous Multicomputers," ACM (1989) (51056DOC020947 - 958)
	ET	Bell, "Ultracomputers: A Teraflop Before Its Time," Communications of the ACM, (August 1992) pp. 27-47 (51056DOC020903 - 923)
	EU	Broomell et al., "Classification Categories and Historical Development of Circuit Switching Topologies," Computing Surveys, Vol. 15, No. 2, pp 95-133 (June 1983) (51056DOC033002 - 040)
	EV	Culler et al., "Analysis of Multithreaded Microprocessors Under Multiprogramming," Report No. UCB/CSD 92/687 (May 1992) (51056DOC069283 - 300)
	EW	D'Inovan et al., "Pixel Processing in a Memory Controller," IEEE Computer Graphics and Applications, pp. 51-61 (January 1995) (51056DOC059635 - 645)
	EX	Fields, "Hunting for Wasted Computing Power: New Software for Computing Networks Puts Idle PC's to Work," Univ. of Wisconsin-Madison, http://www.cs.wisc.edu/condor/doc/Wiscldea.html (1993) (51056DOC068704 - 711)
	EY	Grist, "Cluster Computing: The Wave of the Future?," Oak Ridge National Laboratory, 84OR21400 (May 30, 1994) (51056DOC020924 - 929)
	EZ	Ghafoor, "Systolic Architecture for Finite Field Exponentiation," IEEE Proceedings, Vol. 136 (November 1989) (51056DOC071700 - 705)
	FA	Giloi, "Parallel Programming Models and their Interdependence with Parallel Architectures," IEEE Proceedings (September 1993) (51056DOC071792 - 801)
	FB	Hwang et al., "Parallel Processing for Supercomputers and Artificial Intelligence," (1993) (51056DOC059663 - 673)
	FC	Hwang, "Advanced Computer Architecture: Parallelism, Scalability, Programmability," (1993) (51056DOC059656 - 662)
	FD	Hwang, "Computer Architecture and Parallel Processing," McGraw Hill (1984) (51056DOC070166 - 1028)
	FE	Iwaki, "Architecture of a High Speed Reed-Solomon Decoder," IEEE Consumer Electronics (January 1994) (51056DOC071687 - 694)
	FF	Jain et al., "Square-Root, Reciprocal, SINE/COSINE, ARCTANGENT Cell for Signal and Image Processing," IEEE ICASSP '94, pp. II-521 - II-524 (April 1994) (51056DOC003070 - 073)
	FG	Loudon et al., "Architectural and Implementation Tradeoffs in the Design of Multiple-Context Processors," Technical Report: CSL-TR-92-523 (May 1992) (51056DOC069301 - 327)
	FH	Lawrie, "Access and Alignment of Data in an Array Processor," IEEE Transactions on Computers, Vol. C-24, No. 12, pp. 99-109 (December 1975) (51056DOC002932 - 942)
	FI	Le-Ngoc, "A Gate-Array-Based Programmable Reed-Solomon Codec: Structure-Implementation-Applications," IEEE Military Communications (1990) (51056DOC071695 - 699)
	FJ	Litzkow et al., "Condor - A Hunter of idle Workstations" JBBR (1988) (51056DOC068712 - 719)
	PK	Markstein, "Computation of Elementary Functions on the IBM RISC System/6000 Processor," IBM J. Res. Develop., Vol. 34, No. 1, pp 111-19 (January 1990) (51056DOC059620 - 628)
↓	FL	Nieahus, "A Fast Square Rooter Combining Algorithmic and Table Lookup Techniques," IEEE Proceedings Southeastcon, pp. 1103-05 (1989) (51056DOC061469 - 471)
DW	PM	Renwick, "Building a Practical HIPPI LAN," IEEE, pp. 355-60 (1992) (51056DOC020937 - 942)

Examiner Signature	/Daniel Washburn/	Dated Considered	08/18/2006
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Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	10/616,303
				Filing Date	July 10, 2003
				First Named Inventor	Craig Hansen
				Group Art Unit	2676
				Examiner Name	Mackly Monestini
Sheet	8	of	10	FAX RECEIVED	
OFFICE OF PETITIONS					
Attorney Docket Number 43876-144					

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS					
		Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issued number(s), publisher, city and/or country where published.			
Examiner Initials*	Cite No. ¹				
DW	FN	Rohrbacher et al., "Image Processing with the Staran Parallel Computer," IEEE Computer, Vol. 10, No. 8, pp. 54-59 (August 1977) (reprinted version pp. 119-124) (51056DOC002943 - 948)			
	FO	Ryne, "Advanced Computers and Simulation," IEEE, pp. 3229-33 (1993) (51056DOC020883 - 887)			
	FP	Siegel, "Interconnection Networks for SIMD Machines," IEEE Computer, Vol. 12, No. 6 (June 1979) (reprinted version pp. 110-118) (51056DOC002949 - 957)			
	FQ	Singh et al., "A Programmable HIPPI Interface for a Graphics Supercomputer," ACM (1993) (51056DOC020888 - 896)			
	FR	Smith, "Cache Memories," Computing Surveys, Vol. 14, No. 3 (September 1982) (51056DOC071586 - 643)			
	FS	Tenbrink et al., "HIPPI: The First Standard for High-Performance Networking," Los Alamos Science (1994) (51056DOC020943 - 946)			
	FT	Tolmie, "Gigabit LAN Issues: HIPPI, Fibre Channel, or ATM," Los Alamos National Laboratory Report No. LA-UR-94-3994 (1994) (51056DOC046599 - 609)			
	FU	Tolmie, "HIPPI: It's Not Just for Supercomputers Anymore," Data Communications (May 8, 1995) (51056DOC071802 - 809)			
	FV	Toyokura et al., "A Video DSP with a Macroblock-Level-Pipeline and a SIMD Type Vector-Pipelined Architecture for MPEG2 CODEC," ISSCC94, Section 4, Video and Communications Signal Processors, Paper WP 4.3, pp. 74-75 (1994) (51056DOC003659 - 660)			
	FW	Tulisen et al., "Simultaneous Multithreading: Maximizing On-Chip Parallelism," Proceedings of the 22nd Annual International Symposium on Computer Architecture (June 1995) (51056DOC071434 - 443)			
	FX	Turcotte, "A Survey of Software Environments for Exploiting Networked Computing Resources," Engineering Research Center for Computational Field Simulation (June 11, 1993) (51056DOC069098 - 256)			
	FY	Vetter et al., "Network Supercomputing: Connecting Cray Supercomputers with a HIPPI Network Provides Impressively High Execution Rates," IEEE Network (May 1992) (51056DOC020930 - 936)			
	FZ	Wang, "Bit-Level Systolic Array for Fast Exponentiation in GF(2 ^m)," IEEE Transactions on Computers, Vol. 43, No. 7, pp. 838-41 (July 1994) (51056DOC059407 - 410)			
↓	GA	Ware et al., "64 Bit Monolithic Floating Point Processor," IEEE Journal of Solid-State Circuits, Vol. Sc-17, No. 5 (October 1982) (51056DOC039646 - 655)			
	GB	"Bit Manipulator," IBM Technical Disclosure Bulletin, pp. 1575-76 (November 1974) (51056DOC010205 - 206)			
↓	GC	Finney et al., "Using a Common Barrel Shifter for Operand Normalization, Operand Alignment and Operand Unpack and Pack in Floating Point," IBM Technical Disclosure Bulletin, pp. 699-701 (July 1986) (51056DOC010207 - 209)			
	GD	Data General AVIONIC A 550, 550, 4500 and 5500 Servers			
DW	GE	Jovanovic et al., "Computational Science: Advances Through Collaboration," San Diego Supercomputer Center Science Report (1993) (51056DOC068769 - 779)			
↓	GF	High Performance Computing and Communications: Toward a National Information Infrastructure, National Science Foundation (NSF) (1994) (51056DOC068791 - 801)			
↓	GG	National Coordination Office for High Performance Computing and Communications, "High Performance Computing and Communications: Foundation for America's Information Future" (1996) (51056DOC072102 - 243)			
DW	GH	Wilson, "The History of the Development of Parallel Computing," http://ei.cs.vt.edu/~history/Parallel.html (51056DOC068720 - 757)			

Examiner Signature	/Daniel Washburn/	Dated Considered	08/18/2006
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Sheet	9	of	10	Examiner Name	Mackly Monestime
				Attorney Docket Number	43876-144

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No. ³	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.			
DW	GI	IEEE Standard 754 (ANSI/IEEE Std. 754-1985) (31056DOC019304 - 323)			—
		Original Complaint for Patent Infringement, <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed March 26, 2004			—
	GJ	Amended Complaint for Patent Infringement, <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed April 20, 2004			—
	GK	Expert Witness Report of Richard A. Killworth, Esq. <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005			—
	GL	Declaration and Expert Witness Report of Ray Mercer Regarding Written Description and Enablement Issues, <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> , C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12 2005			—
	GM	Corrected Expert Report of Dr. Stephan B. Wicker Regarding Invalidity of U.S. Patent Nos. 5,742,840; 5,794,060; 5,764,061; 5,809,321; 6,584,482; 6,643,765; 6,725,356 and Exhibits A-I; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> , C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 6, 2005			—
	GN	Defendants Intel and Dell's Invalidity Contentions with Exhibits A-G; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 19, 2005			—
	GO	Defendants Dell Inc. and Intel Corporation's Identification of Prior Art Pursuant to 35 USC §282; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 7, 2005			—
	GP	Request for Inter Partes Reexamination Under 35 USC §§ 311-318 of U.S. Patent No. 6,725,356 filed on June 28, 2005			—
	GQ	Deposition of Larry Meanemeyer on September 22, 2005 and Exhibit 501; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division			—
	GR	Deposition of Leslie Kohn on September 22, 2005; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division			—
	GS	Intel Article, "Intel Announces Record Revenue of 9.96 Billion", October 18, 2005			—
	GT	The New York Times Article, "Intel Posts 5% Profit Increase on Demand for Notebook Chips", October 19, 2005			—
↓	GU	USA Today Article, "Intel's Revenue Grew 18% In Robust Quarter for Tech", October 19, 2005			—
↓	GV	The Wall Street Journal Article, "Intel Says Chip Demand May Slow", October 19, 2005			—
DW	GW	The New York Times Article, "Intel Settlement Revives A Fading Chip Designer", October 20, 2005			—

Examiner Signature	/Daniel Washburn/	Dated Considered	08/18/2006
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